AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Withdrawn) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

a conductive member buried in a through hole that goes through the first semiconductor chip;

a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a wiring substrate to which the first semiconductor chip is mounted; and

a third connecting terminal at least portion of which is formed at a position corresponding to one of the first connecting terminal and the second connecting terminal, and which is electrically connected to the one of the first connecting terminal and the second connecting terminal.

2. (Withdrawn) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a first connecting terminal arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element;

a conductive member buried in a through hole that goes through the first semiconductor chip;

a second connecting terminal arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive member;

a lead frame to which the first semiconductor chip is mounted, and at least part of which is arranged at a position facing to one of the first connecting terminal and the second connecting terminal, and which is electrically connected to the one connecting terminal; and

an insulator that seals an inner lead portion of the lead frame and the first semiconductor chip.

3. (Canceled)

4. (Withdrawn) A semiconductor device according to claim 3, wherein, one of the first connecting terminals and the second connecting terminals are arranged to be facing to the assembly board and the average density of arrangement of the one of the first connecting terminals and the second connecting terminals are made lower than that of another of the first connecting terminals and the second connecting terminals.

5. (Withdrawn) A semiconductor device according to claim 4, wherein, a portion of either the first connecting terminals or the second connecting terminals are distributed and arranged on the central area of the semiconductor chip, and power source supply potential or ground potential are to be applied thereto.

6. (Withdrawn) A semiconductor device according to claim 1, further comprising a bonding wire configured to connect at least portion of the connecting terminal that is not used for flip-chip connection with the wiring substrate of the first connecting terminal and the second connecting terminal in the first semiconductor chip with the third connecting terminal formed on the wiring substrate.

7. (Withdrawn) A semiconductor device according to claim 2, further comprising a bonding wire configured to connect at least portion of the connecting terminal that is not used for flip-chip connection with the lead frame of the first connecting terminal and the second connecting terminal in the first semiconductor chip with an inner lead portion of the lead frame.

8. (Withdrawn) A semiconductor device according to claim 1, further comprising a second semiconductor chip stacked on the first semiconductor chip, wherein at least portion of the connecting terminal that is not used for flip-chip connection with the wiring substrate of the first connecting terminal and the second connecting terminal in the first semiconductor chip is coupled to the second semiconductor chip.

9. (Withdrawn) A semiconductor device according to claim 1, further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above the first semiconductor chip, wherein at least portion of the connecting terminal that is not used for flip-chip connection with the wiring substrate of the first connecting terminal and the

second connecting terminal in the first semiconductor chip is coupled to the second to n-th semiconductor chips.

10. (Withdrawn) A semiconductor device according to claim 2, further comprising a second semiconductor chip stacked on the first semiconductor chip, wherein at least portion of the connecting terminal that is not used for flip-chip connection with the lead frame of the first connecting terminal and the second connecting terminal in the first semiconductor chip is coupled to the second semiconductor chip.

11. (Withdrawn) A semiconductor device according to claim 2, further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above the first semiconductor chip, wherein at least portion of the connecting terminal that is not used for flip-chip connection with the lead frame of the first connecting terminal and the second connecting terminal in the first semiconductor chip is coupled to the second to n-th semiconductor chips.

12. (Canceled)

13. (Canceled)

14. (Withdrawn) A semiconductor device according to claim 8, further comprising a bonding wire configured to connect at least portion of the plurality of connecting terminals of the semiconductor chips to be stacked with each other.

15. (Withdrawn) A semiconductor device according to claim 10, further comprising a bonding wire configured to connect at least portion of the plurality of connecting terminals of the semiconductor chips to be stacked with each other.

16. (Withdrawn) A semiconductor device according to claim 12, further comprising a bonding wire configured to connect at least portion of the plurality of connecting terminals of the semiconductor chips to be stacked with each other.

17. (Withdrawn) A semiconductor device according to claim 8, further comprising a conductive bump configured to connect at least portion of the plurality of connecting terminals of the semiconductor chips to be stacked with each other.

18. (Withdrawn) A semiconductor device according to claim 10, further comprising a conductive bump configured to connect at least portion of the plurality of connecting terminals of the semiconductor chips to be stacked with each other.

19. (Canceled)

20. (Canceled)

21. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a plurality of first connecting terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element, the first connecting terminals having substantially the same configuration;

a plurality of conductive members buried in a plurality of through holes that go through the first semiconductor chip; and

a plurality of second connecting terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive members,

wherein at least either the first connecting terminals or the second connecting terminals is coupled to an assembly board, and

some of the first connecting terminals or the second connecting terminals are distributed and arranged substantially on an entire surface of the semiconductor chip, and a power source supply potential or ground potential is to be applied to said some of the first or second connecting terminals.

22. (Previously Presented) A semiconductor device according to claim 21, further comprising a second semiconductor chip stacked on the first semiconductor chip, wherein at least portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the

second connecting terminals in the first semiconductor chip is coupled to the second semiconductor chip.

23. (Currently amended) A semiconductor device according to claim 21, further comprising a second to an n-th (wherein n is a positive integer of three or more) semiconductor chips stacked above first semiconductor chip, wherein at least a portion of the connecting terminals arranged on a stacked surface between the first semiconductor chip and the second semiconductor chip of the first connecting terminals and the second connecting terminals in the first semiconductor chip is coupled to the second to n-th semiconductor chips.

24. (Previously Presented) A semiconductor device according to claim 22, wherein said at least a portion of the plurality of connecting terminals comprises conductive bumps.

25. (Currently Amended) A semiconductor device comprising:

a first semiconductor chip where a semiconductor element is formed;

a plurality of first connecting ~~terminal~~ terminals arranged on a semiconductor element formation surface side in the first semiconductor chip, and connected electrically to the semiconductor element, the first connecting terminals having substantially the same configuration;

a plurality of conductive ~~member~~ members buried in a through hole that goes through the first semiconductor chip;

a plurality of second connecting ~~terminal~~ terminals arranged on a back surface side of the semiconductor element formation surface in the first semiconductor chip, and connected electrically to the semiconductor element via the conductive ~~member~~ members;

a second semiconductor chip stacked on the first semiconductor chip;

a plurality of third connecting ~~terminal~~ terminals arranged on a semiconductor element formation surface side in the second semiconductor chip,

wherein one of the first connecting ~~terminal~~ terminals and the second connecting ~~terminal~~ terminals of the first semiconductor chip is arranged at a position facing the third connecting ~~terminal~~ terminals of the second semiconductor chip, the first semiconductor chip and the second semiconductor chip are electrically connected with each other through the facing connecting terminals,

the second semiconductor chip is thicker or larger than the first semiconductor chip, and

~~a portion of either~~ some of the first connecting terminals or the second connecting terminals ~~is~~ are distributed and arranged substantially on an entire surface of the semiconductor chip, and a power source supply potential or ground potential is to be applied to said ~~portion~~ some of the first or second connecting terminals.